

FIG.11

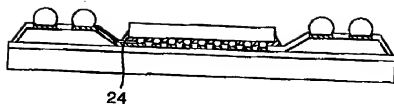


FIG.12

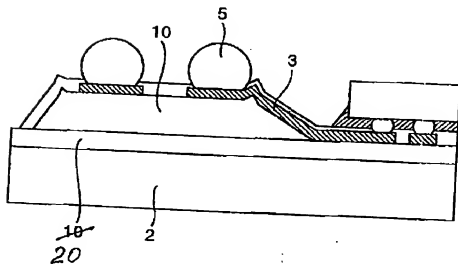


FIG.23A

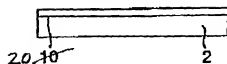


FIG.23B

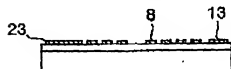


FIG.23C

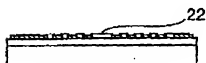


FIG.23D

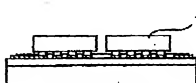


FIG.23E

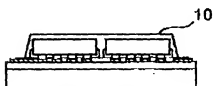


FIG.23F

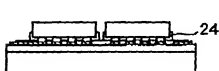


FIG.23G



FIG.27

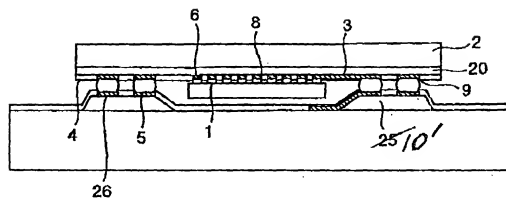


FIG.28

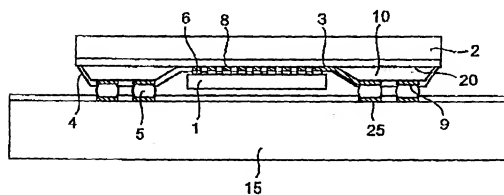


FIG.39A

RELEASED BY  
EJECTER PIN

THE STRESS COMPLIANT  
LAYER FORMED SILICON  
SUBSTRATE

FIG.39B

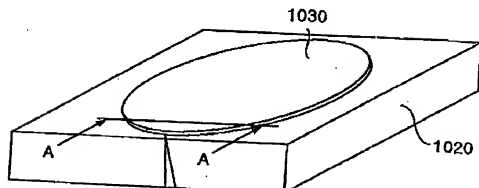


FIG.39C

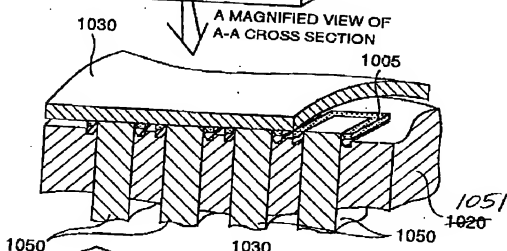


FIG.39D

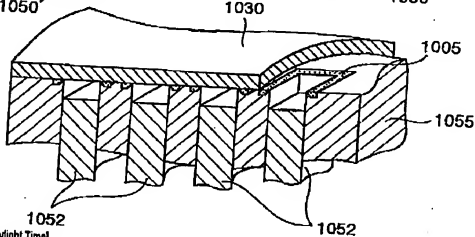


FIG. 42A

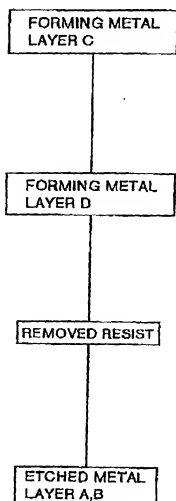


FIG. 42B

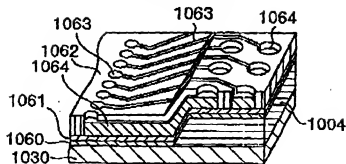


FIG. 42C

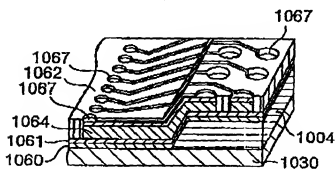


FIG. 42D

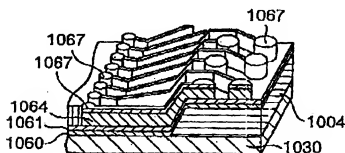


FIG. 42E

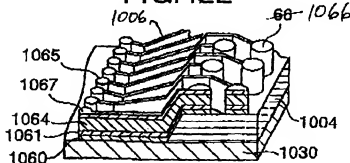


FIG.45A

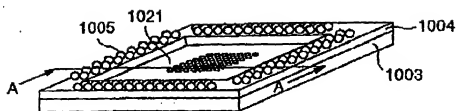


FIG.45B

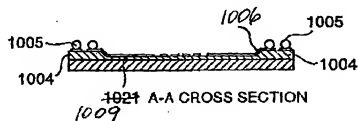


FIG.46A

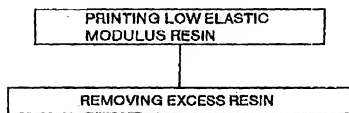


FIG.46B

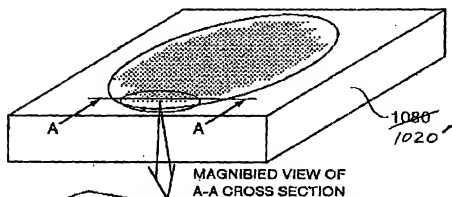


FIG.46C

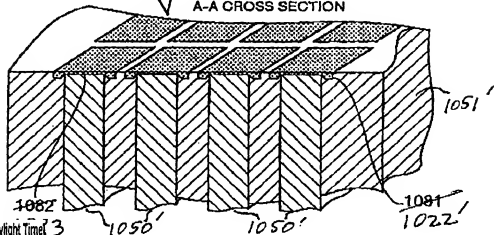


FIG.47A

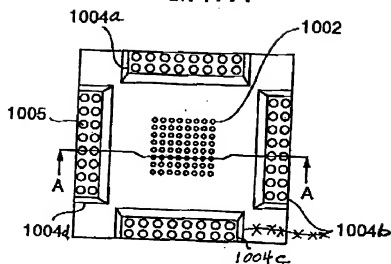


FIG.47B



FIG.48

